WHAT IS CLAIMED IS:

1. A method of forming a thin film transistor (TFT) structure, said method comprising the steps of:

providing a substrate having a first surface and a second surface;

forming a plurality of stacked structures on said first surface of said substrate, each stacked structure including a first conducting layer, an insulation layer, an amorphous silicon layer, and an ohmic contact layer;

forming a patterned photo-imagable layer between said plurality of stacked structures;

forming a second conducting layer on said patterned photo-imagable layer and said ohmic contact layer;

patterning said second conducting layer and said ohmic contact layer to expose said amorphous silicon layer, wherein a source electrode and a drain electrode are formed;

forming a passivation layer on said amorphous layer and said second conducting layer; and

forming a transparent electrode on said passivation layer and electrically connecting to said second conducting layer.

2. The method according to claim 1, wherein said plurality of stacked structures are formed in one step of photolithography.

3. The method according to claim 1, wherein said substrate is exposed from said second surface by using said plurality of stacked structure as masks in said step of forming a patterned photo-imagable layer.

4. The method according to claim 1, wherein said first conducting layer is a gate electrode.

5. A method of forming a thin film transistor (TFT) structure, said method comprising the steps of:

providing a substrate having a first surface and a second surface;

forming a plurality of first pre-stacked structures and a plurality of second pre-stacked structures on said first surface of said substrate, each first pre-stacked structure including a first conducting layer, an insulation layer, an amorphous silicon layer, an ohmic contact layer, and a photoresist layer having a first thickness, each second pre-stacked structure including said first

conducting layer, said insulation layer, said amorphous silicon layer, an ohmic contact layer, and a photoresist layer having a second thickness, wherein said second thickness is less than said first thickness;

removing said photoresist layer having said second thickness to expose said plurality of second pre-stacked structures;

removing said ohmic contact layer and said amorphous silicon layer of said plurality of second pre-stacked structures to form a plurality of first stacked structures and a plurality of second stacked structures, wherein said plurality of first stacked structures includes said first conducting layer, said insulation layer, said amorphous silicon layer and said ohmic contact layer, and said plurality of second stacked structures at least includes said first conducting layer;

forming a patterned photo-imagable layer between said plurality of first stacked structures and said plurality of said second stacked structures, wherein said substrate is exposed from said second surface by using said plurality of first stacked structures and said plurality of said second stacked structures as masks;

forming a second conducting layer on said patterned photo-imagable layer, said plurality of first stacked structures, and said plurality of said second

stacked structures;

patterning said second conducting layer to expose a part of said amorphous silicon layer of said plurality of first stacked structures;

forming a passivation layer on said amorphous silicon layer of said plurality of first stacked structure, said first conducting layer of said plurality of second stacked structure, and said second conducting layer of said plurality of first stacked structure; and

forming a transparent electrode on said passivation layer of said plurality of first stacked structure and said plurality of second stacked structure, wherein a first portion of said transparent electrode electrically connects to one of said source electrode and drain electrode, and a second portion of said transparent electrode electrically connects said second conducting layer of said plurality of first stacked structures and said first conducting layer of said plurality of second stacked structures.

6. The method according to claim 5, wherein said plurality of first stacked structures and said plurality of said second stacked structures are formed using one step of photolithography.

7. The method according to claim 5, wherein said substrate is exposed

from said second surface by using said plurality of first stacked structures and said plurality of second stacked structures as masks in said step of forming a patterned photo-imagable layer.

8. The method according to claim 5, wherein said first conducting layer is a gate electrode.

9. A thin film transistor (TFT) structure, comprising:

a plurality of stacked structures on a substrate, said plurality of stacked structures including a first conducting layer, an insulation layer, an amorphous silicon layer and an ohmic contact layer;

a photo-imagable layer between said plurality of stacked structures;

a source electrode and a drain electrode on said photo-imagable layer, wherein said source electrode is connected to a portion of said amorphous silicon layer and said drain electrode is connected to another portion of said amorphous silicon layer;

a passivation layer on said amorphous silicon layer, said source electrode and said drain electrode; and

a transparent electrode on said passivation layer and electrically

connected to one of said source electrode and said drain electrode.

10. The TFT structure according to claim 9, wherein said plurality of stacked structures are formed by one mask manufacturing.

11. The TFT structure according to claim 9, wherein said first conducting layer is a gate electrode.

12. The TFT structure according to claim 9, wherein each said source electrode and said drain electrode comprise a second conducting layer and an ohmic contact layer, said second conducting layer is positioned between said amorphous silicon layer and said passivation layer, said ohmic contact layer is positioned between said amorphous silicon layer and said second conducting layer, such that said second conducting layer connects to said amorphous silicon layer through said ohmic contact layer.

13. A thin film transistor (TFT) structure, comprising:

a plurality of first stacked structures and a plurality of second stacked structures on a substrate, wherein each first stacked structure includes a first conducting layer, an insulation layer, an amorphous silicon layer and an ohmic contact layer, and each second stacked structure at least includes said first conducting layer;

a photo-imagable layer between said plurality of first stacked structures and said plurality of said second stacked structures;

a source electrode and a drain electrode on said photo-imagable layer and said plurality of first stacked structures;

a passivation layer on said photo-imagable layer and said source electrode and said drain electrode; and

a transparent electrode on said passivation layer wherein a first portion of said transparent electrode electrically connects to one of said source electrode and drain electrode, and a second portion of said transparent electrode electrically connects said second conducting layer of said plurality of first stacked structures and said first conducting layer of said plurality of second stacked structure.

14. The TFT structure according to claim 13, wherein said plurality of first stacked structures and said plurality of second stacked structures are formed by one mask manufacturing.

15. The TFT structure according to claim 13, wherein each said source electrode and said drain electrode comprise a second conducting layer and an ohmic contact layer, said second conducting layer is positioned under said

passivation layer, said ohmic contact layer is positioned between said amorphous silicon layer and said second conducting layer, such that said second conducting layer connects to said amorphous silicon layer of said plurality of first stacked structures through said ohmic contact layer.

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